A Novel Nonvolatile Memory with Spin Torque Transfer Magnetization Switching: Spin-RAM

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Abstract

A novel nonvolatile memory utilizing spin torque transfer magnetization switching (STS), abbreviated Spin-RAM hereafter, is presented for the first time. The Spin-RAM is programmed by magnetization reversal through an interaction of a spin momentum-torque-transferred current and a magnetic moment of memory layers in magnetic tunnel junctions (MTJs), and therefore an external magnetic field is unnecessary as that for a conventional MRAM. This new programming mode has been accomplished owing to our tailored MTJ, which has an oval shape of 100 x 150 nm. The memory cell is based on a 1-Transistor and a 1-MTJ (1T1J) structure. The 4kbit Spin-RAM was fabricated on a 4 level metal, 0.18 μm CMOS process. In this work, writing speed as high as 2 ns, and a write current as low as 200 μA were successfully demonstrated. It has been proved that Spin-RAM possesses outstanding characteristics such as high speed, low power and high scalability for the next generation universal memory.

Introduction

A conventional MRAM, which is equipped with high speed and endurance free properties, is an attractive candidate for a nonvolatile RAM. It uses current induced magnetic field for write operation and it is proportional to the demagnetization field which is increases as decreasing magnetic tunnel junction (MTJ) size (1, 2), thus it was pointed out that there are difficulties in write power consumption and scaling. To solve these problems, we introduced new spin torque transfer magnetization switching (STS) system which has every possibility of overcoming the obstacles of their difficulties. The simplified STS procedure is explained in Fig.1.

Although STS is quite a new technology, which was predicted theoretically in 1996 (3, 4) and observed experimentally in 1998 (5, 6), and should need more fundamental investigations for understanding the detail, we decided to fabricate the Spin-RAM to show by means of evidence that the Spin-RAM has been equipped with distinguished properties as follows. The direct injection of spin polarized electron can efficiently reverse the direction of the magnetic layer comparing to a current induced magnetic field. Then, lower power operation should definitely be expected. Also, once a switching current density meets a specification at a certain technology node, required STS current should scalably decrease for smaller nodes.

In the Spin-RAM cell structure, an MTJ is connected in series with a transistor, then, applicable current is limited less than some hundreds of μA. Switching current order of mA is far beyond Spin-RAM operation. That is the one of the reason why STS development is still limited to feasibility studies. In this work, we have successfully reduced a switching current due to our tailored MTJ structure and materials. Besides, the 4kbit Spin-RAM has worked evidently for the first time, high speed and low power operations were also demonstrated. According to STS characteristics, smaller MTJ size is desirable for the Spin-RAM. A future prospect of the Spin-RAM for a smaller node is estimated, and the promising characteristics have been recognized confidently.

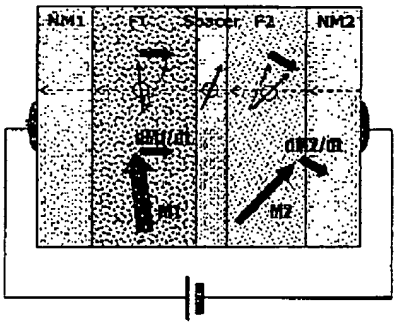

Figure 1 A schematic image of a procedure of spin torque transfer switching (STS). An STS element has two ferromagnetic layers, F1 and F2, and a spacer layer between F1 and F2. In this work, an MTJ is composed of a pinned layer (F1), an MgO tunnel barrier layer (Spacer) and a free magnetic layer (F2). When a spin polarized electron flows from F2 to F1, the spin direction rotates according to the directions of magnetic moment M_1 and M_2 (1). The rotation of spin direction of the electrons in F1 and F2 layer are the origin of a spin torque, dM_1/dt and dM_2/dt, to the magnetic moment M_1 and M_2. The given torque is large enough, magnetization of F2, M_2, is reversed. Then, the magnetization of F1 and F2 transform from parallel to anti-parallel alignment (From low resistance state to high resistance state).

Memory cell structure and process integration

The difference between a Spin-RAM and a conventional MRAM is only in write operation mechanism, and read system is the same. A memory cell of the Spin-RAM is composed of a transistor, an MTJ, a word line (WL), a bit line (BL) and a source line (SL), as shown in Fig. 2 (a). An MTJ has two magnetic layers and a tunnel barrier layer between them. One of the magnetic layers is switching layer, and the other is pinned its magnetization direction. A tunnel barrier layer is made of crystallized MgO whose thickness is controlled less than 1nm for the proper resistance area (RA) product of the MTJ. For the memory characterizations, cell array was designed, shown in Fig. 2 (b). On the write operation, a WL is selected, and positive voltage is applied on a BL or a SL of a selected column. The magnetization direction of a switching layer is controlled by the current direction. On the read operation, a WL is selected, and voltage of ~0.1 V is applied on a BL of a selected column. Write and read properties were investigated both by voltage sweep mode and by pulse mode.

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Exhibit I

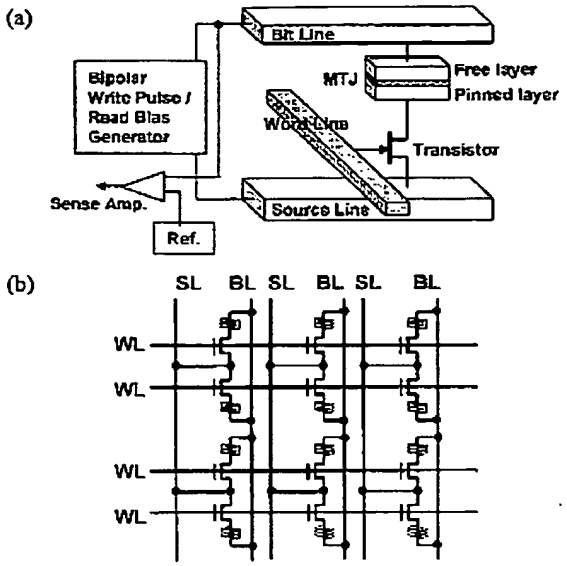

Figure 2 (a) A schematic memory cell image, and (b) cell array image. To control current direction, voltage is applied on a bit line (BL) or a source line (SL) on the write operation.

The Spin-RAM device was fabricated by using 0.18 μm CMOS technologies with a 4 level metal. Cross-sectional SEM and TEM images indicate our process integration and structure of the 4kbit Spin-RAM device, as shown in Fig. 3. We have developed a novel MTJ with our original CoFeB ferromagnetic layer (7) and an MgO tunnel barrier layer. Although an MTJ is used in the MRAM, additional development is needed for the Spin-RAM devices. The main concern is an improvement of spin torque transfer efficiency. Figure 4 shows a cross-sectional TEM image of an MTJ film. To obtain a higher tunneling spin polarization and a lower RA product, a crystal growth condition of (100) oriented thin MgO tunnel barrier layer and microstructure of magnetic materials have been optimized. As a result, magnetoresistance (MR) ratio more than 160% at RA product of 20 $\Omega\mu m^2$ was

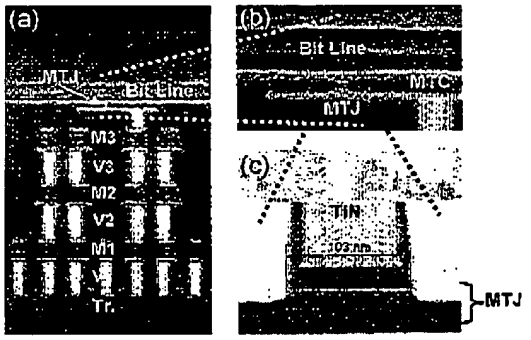

Figure 3 (a) and (b) Cross-sectional SEM images showing the Spin-RAM module integrated between a bypass line and a bit line. (c) A cross- sectional TEM image showing the etched TiN hard mask and MTJ. An MTJ is placed between bit lines and bypass lines by using borderless contact process (2).

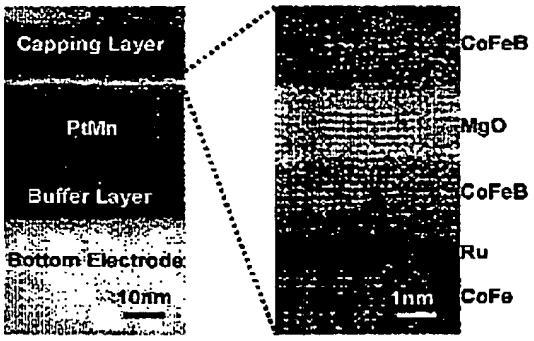

Figure 4 A cross-sectional TEM images showing MTJ film stack and (100) oriented MgO barrier layer. The MTJ film has a PtMn for an anti-ferromagnetic (AF) pinning layer, a CoFe/Ru/CoFeB for a synthetic anti-ferromagnetic (SAF) pinned layer, MgO for a tunnel barrier layer, and CoFeB for a free layer.

obtained. An MTJ patterning process has been developed based on EB lithography technologies in order to obtain a minimum MTJ size of 100 x 150 nm in an oval shape. To elucidate MTJ shape effect, MTJs with different sizes and aspect ratios were processed. MTJ sizes were checked by SEM images after MTJ etching process.

Spin-RAM Chip characteristics

Typical *I-V* curve and *R-V* curve are obtained through the voltage sweep mode, as shown in Fig. 5. Resistance was changed at the positive and the negative threshold voltages. On the high state region, the *I-V* curve was not linear, and on the *R-V* curve, cell resistance was decreased with increasing the applied voltage. This is caused by a tunnel magnetoresistance (TMR) effect.

Figure 6 shows read distributions of the 4kbit circuit, and separation between low state and high state resistance. A good separation was obtained due to the improved MR ratio by the

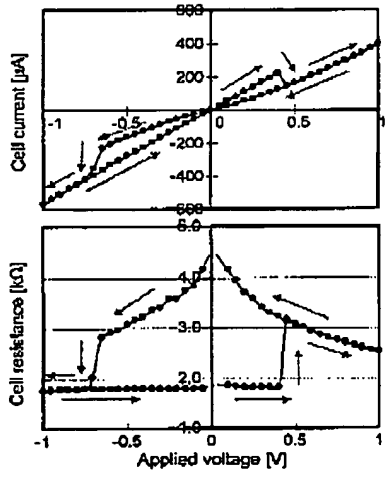

Figure 5 Typical *I-V* and *R-V* curves in voltage sweep mode. When the voltage is applied on a source line, indicating positive applied voltage region, low state resistance switches to high state resistance, and the voltage is applied on a bit line, indicating negative applied voltage region, resistance switches the other way.

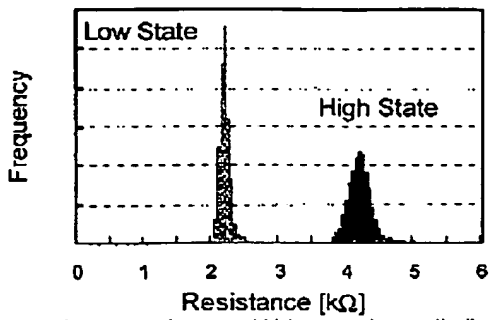

Figure 6 Low state resistance and high state resistance distributions of the 4kbit circuit with MTJ size of 120 x 170 nm. Bias voltage is kept at -0.1 V.

admirably optimized MTJ film, and this result indicates that a parasitic transistor resistance is not a crucial issue. Although the high state resistance and the low state resistance distribution look different, one sigma of both high and low state resistance distributions, σ, was 4% approximately. The distribution will be suppressed less than 1-2% using conventional MRAM production technologies (2).

Write threshold voltage and its distribution are shown in Fig. 7. The average threshold voltage was approximately -0.8V and 1.2V at 100ns current pulse. Improvement of STS efficiency and reduction of a RA product in an MTJ are effective for the reduction of the write threshold voltage. Although the voltage distribution of switching from high to low state is narrower than the other, we do not have the reason at the moment. The switching characteristics have to be further investigated for the reduction of the distribution.

Figure 8 shows write characteristics dependence on MTJ size. Smaller MTJ showed less switching voltage. On the positive voltage, as resistance changes from low state to high state, on-resistance of the transistor is much affected by the MTJ size.

Pulse width dependence on the switching current is shown in Fig. 9. We observed the most MTJs switched within 2 ns pulse. In negative voltage MTJs switched even at 1ns, whereas the applied voltage limited switching in positive region. High speed write operation is demonstrated clearly. As reducing pulse width, switching current increased continuously. Pulse width between 1 ms and 10 ns, a relationship between the switching current and the pulse width was agreed with the theoretical equation of magnetization reversal (8, 9);

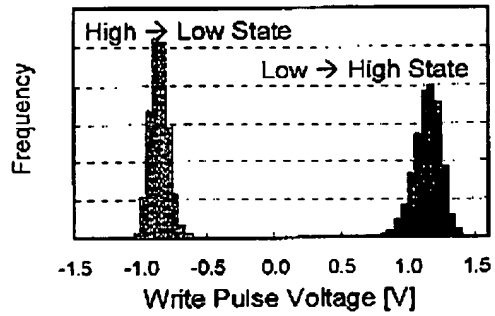

Figure 7 Write voltage distribution of the 4kbit circuit with MTJ size of 120 x 170nm on the 100 ns pulse mode. Positive voltage indicates that the voltage applied on the source line, while negative voltage indicates that the voltage applied on the bit line.

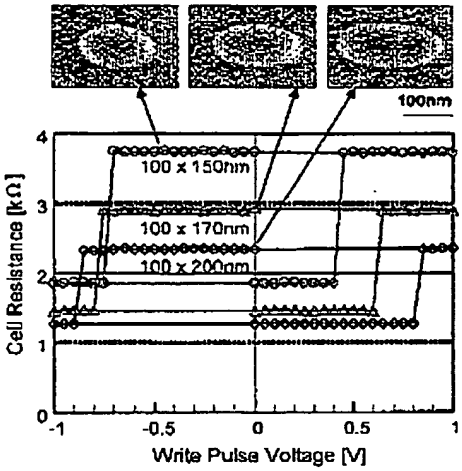

Figure 8 *R-V* curves measured in 1 ms pulse. On the positive voltage, resistance changes from low state to high state, and the other way on the negative voltage. SEM images showing patterned resist using EB lithography, MTJ size of 100x150 nm, 100x170 nm, 100x200 nm. An influence of transistor on the switching characteristics can be reduced by decreasing MTJ sizes.

$$Ic = Ic_0\left\{1-\left(\frac{kT}{E}\right)\ln\left(\frac{\tau}{\tau_0}\right)\right\}, \qquad (1)$$

which is indicated as dotted lines in Fig. 9. Here, Ic : critical switching current, Ic_0 : critical switching current at 0K, E : barrier height, τ : switching time, τ_0 : inverse of the attempt frequency. Below 10 ns, switching current increased rapidly. In this region, switching might be affected by the spin precession. On the other hand, quite a low write threshold current of 200 μA was obtained in the 1ms pulse. This indicates 1/30 reduction of the write current compared to that of a conventional MRAM (1), although relatively long pulse width.

To study the switching behavior, switching probability at each applied current was investigated, as shown in Fig. 10. The switching probability was calculated from 1000 cycle measurements on each current step. Calculated probability was shown as dots in Fig. 10. From the theoretical point of view, since magnetization reversal is dependent on magnetic

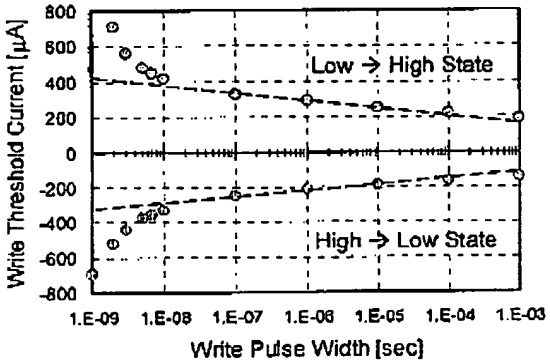

Figure 9 Switching currents on the different pulse width. MTJ size of 115x155 nm. Threshold currents were averaged from 50 cycle measurements on each pulse width. As write pulse width is reduced, both write threshold current and current distributions were increased.

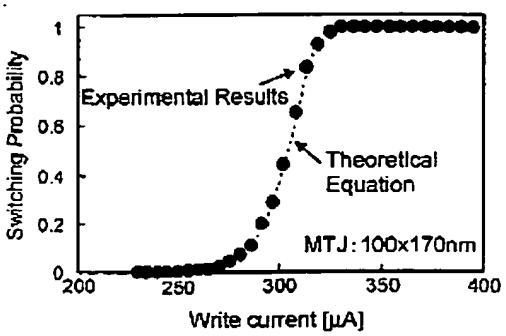

Figure 10 A switching probability at each applied current was investigated by both experiment (circle) and theoretical estimation (dotted line). For the probability estimation, 1000 cycle measurements were performed on each current step.

memorizing energy (Δ), switching probability is expressed as the following equation (8, 9),

$$P_{sw} = 1 - \exp\left\{-\frac{t}{\tau_0}\exp\left[-\Delta_0\left(1-\frac{I}{Ic_0}\right)\right]\right\}. \qquad (2)$$

Here, Δ_0 magnetic memorizing energy without any current and magnetic field, and t is pulse width. A dashed line indicates a calculation result from the equation. STS result on our Spin-RAM circuit is consistent with the magnetization switching theory (8, 9).

Endurance test was performed, as shown in Fig.11. The MTJ resistance shows accurate two values, corresponding to the two magnetization direction of the switching layer. In case the 10^{12} cycles of 100 ns pulse width, resistance both high and low state were stable during the test, although high state resistance has 4% dropped at the end of the test. This preliminary result suggests that the Spin-RAM has good reliability for write/erase cycle, however, more intensive investigations will be required to ensure the production level reliability.

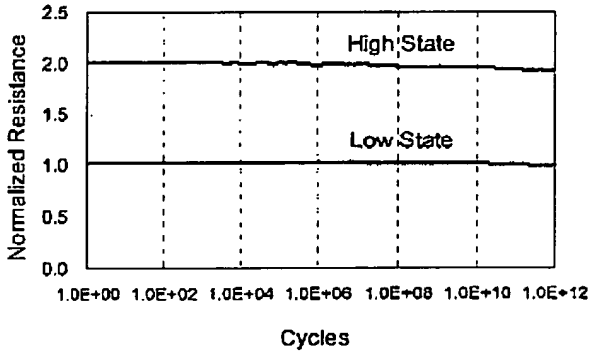

Figure 11 Resistance change during 10^{12} cycle test in 100 ns pulse width. Resistance was normalized by a low state resistance in the first cycle. STS was reproducible during the cycle test.

Finally, we have considered the scaling capability of Spin-RAM. As we have described in the chip results, the switching behavior of the Spin-RAM are well characterized by switching current (Ic) and magnetic memorizing energy (Δ). Both are simplified as follows.

$$Ic = A \cdot Ms^2 \cdot V \qquad (3)$$

$$\Delta = B \cdot Hc_0 \cdot Ms \cdot V \qquad (4)$$

A and B are constant, Ms is magnetic material parameter, Hc_0 is anisotropic magnetic energy, and V is volume of switching layer. As MTJ size decreases, which is equivalent to smaller V, Hc_0 value increases. Then, Ic is reduced with maintaining a certain amount of Δ. From this work, a switching current of approximately 400 μA in 10ns was obtained. In case of a smaller MTJ size of 50 x 100nm, which is suitable for 45nm design rule, an estimated switching current can be decreased to 140μA in 10ns. Furthermore, smaller MTJs will be able to reduce write current according to the theory. We have already made smaller size MTJ test elements down to 40 x 90nm, and confirmed its good STS characteristics. This excellent scaling possibility is one of the most attractive features of the Spin-RAM.

Conclusion

A new nonvolatile memory with STS was demonstrated for the first time. In an integrated Spin-RAM circuit, high speed switching within 2 ns pulse was confirmed. As theoretical predictions agreed well with the switching experiment, it is proved that the switching driving force is derived from the spin polarized current, not from heat-up assist or current induced field. Then, theoretical predictions can facilitate a practical memory design. Reliability of MgO tunnel barrier was also confirmed through the 10^{12} cycle test. It has been proved that the nonvolatile Spin-RAM has equipped with distinguished properties such as high speed, low power and high scalability.

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